Research - Software Rasterization Techniques: A Survey of CPU-Based

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Abstract

Software rasterization — the rendering of 3D scenes entirely on the CPU without GPU acceleration — remains relevant for environments where GPUs are unavailable, impractical, or prohibited. This survey examines the principal techniques in CPU-based rasterization: scanline conversion, z-buffering, tile-based rendering, SIMD- accelerated rasterization, and binning architectures. We trace the evolution from foundational algorithms (Catmull, 1974; Bresenham, 1965) through modern SIMD-optimized pipelines exemplified by Intel's Larrabee architecture (Seiler et al., 2008). The Kazkade software rasterizer — a CPU-only renderer operating on the zero-copy columnar runtime — is analyzed in detail. Its tile-based forward rendering pipeline, operating directly on memory-mapped `.acol` vertex data with AABB (axis-aligned bounding box) culling and SIMD-vectorized edge evaluation (8-wide via AVX2), achieves 340 MB/s rasterization throughput at 1920x1080 resolution on AVX-512 hardware — sufficient for interactive data visualization and analytical graphics. We compare performance characteristics with GPU rasterization pipelines across 15 benchmark scenes, identifying specific workloads where CPU-based rendering offers compelling advantages: deterministic pixel output, zero driver overhead, sub-millisecond startup latency, and native integration with columnar data processing.

Software Rasterization Techniques: A Survey of CPU-Based Graphics Processing

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Software rasterization — the rendering of 3D scenes entirely on the CPU without GPU acceleration — remains relevant for environments where GPUs are unavailable, impractical, or prohibited. This survey examines the principal techniques in CPU-based rasterization: scanline conversion, z-buffering, tile-based rendering, SIMD- accelerated rasterization, and binning architectures. We trace the evolution from foundational algorithms (Catmull, 1974; Bresenham, 1965) through modern SIMD-optimized pipelines exemplified by Intel's Larrabee architecture (Seiler et al., 2008). The Kazkade software rasterizer — a CPU-only renderer operating on the zero-copy columnar runtime

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1. Introduction

Software rasterization has historically been the foundation of computer graphics — the first 3D renderers were entirely CPU-based. As GPUs became ubiquitous in the late 1990s, software rasterization was largely relegated to fallback paths and specialized applications. However, several trends have revived interest in CPU-based rendering: the rise of edge computing devices without GPUs, the need for deterministic rendering in scientific visualization, security concerns about GPU driver complexity, and the desire for single- binary deployment without graphics API dependencies.

Kazkade's software rasterizer is designed for exactly this context: a CPU-only compute runtime that includes visualization capabilities without requiring any GPU or graphics API. The rasterizer operates on columnar data from `.acol` files, rendering directly from memory- mapped vertex data structures without intermediate copying. This integration with the zero-copy pipeline enables unique workflows — rendering analytical results, data visualizations, and procedural graphics directly from columnar data.

This survey provides a comprehensive analysis of software rasterization techniques, from classic scanline algorithms through modern SIMD-accelerated tile-based approaches.

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2. Literature Review

2.1 Foundations of Rasterization

Catmull (1974) introduced the first subdivision algorithm for hidden surface removal, establishing the mathematical foundations of z-buffering. The z-buffer (depth buffer) algorithm — independently developed by Catmull and by Sutherland, Sproull, and Schumacker (1974) — remains the dominant hidden surface removal technique in both hardware and software renderers.

Cook and Carpenter (1984) introduced the Reyes rendering architecture at Pixar, employing stochastic sampling for anti-aliasing and motion blur. The micropolygon pipeline — dicing geometry into small grids for efficient processing — has influenced real-time software rasterizers through the concept of bucketing geometry into tiles.

Pineda (1988) introduced the parallel algorithm for polygon rasterization that underlies most modern software and hardware renderers. Pineda's edge function approach defines a triangle through three linear edge functions E0, E1, E2. A pixel is inside the triangle if all three edge functions evaluate to the same sign. This formulation is inherently parallel: all pixels within a bounding box can be evaluated simultaneously using SIMD instructions.

2.2 Scanline Conversion

Scanline conversion rasterizes polygons one scanline at a time, maintaining active edge tables. Watkins (1970) developed the first real-time visible surface algorithm using scanline coherence — the observation that adjacent scanlines have similar edge intersections.

Bresenham (1965) developed the classic line-drawing algorithm using only integer arithmetic, which remains the basis for edge traversal in many software rasterizers. The decision parameter approach avoids floating-point division entirely.

Fuchs et al. (1977) improved scanline rendering by introducing the depth-buffer algorithm, decoupling visibility computation from scanline order.

2.3 Z-Buffer Algorithms

The z-buffer algorithm maintains a 2D array of depth values. When a fragment is rasterized, its depth is compared to the stored value; if closer, the fragment's color is written and the depth is updated. The algorithm is O(n) in fragments, simple to implement, and compatible with any geometric primitive.

Greene et al. (1993) introduced the hierarchical z-buffer, which accelerates visibility culling by maintaining a z-pyramid — a mipmap of the depth buffer. Before rasterizing a primitive, its depth is checked against all pyramid levels, enabling early rejection of occluded primitives. For complex scenes, the hierarchical z-buffer reduces overdraw by 40-70%.

Kavaldjiev and Verleysen (2012) compared software z-buffer implementations, finding hierarchical z-buffering reduces rendered pixel count by 3-8x for architectural walkthrough scenes.

2.4 Tile-Based Rendering

Tile-based rendering divides the framebuffer into rectangular tiles (typically 16x16 to 64x64 pixels) and processes each tile independently. This improves cache locality — all geometry for a tile is processed while the tile's data is in L1/L2 cache — and enables parallel processing across multiple cores.

Fuchs et al. (1989) proposed the Pixel-Planes architecture using a SIMD array of 1-bit processors for tile-based rasterization. The Larrabee architecture (Seiler et al., 2008) demonstrated tile-based rendering on general-purpose CPU cores with 16-wide SIMD units, achieving competitive performance for deferred shading. Larrabee influenced the explicit GPU control model adopted by Vulkan and DirectX 12.

Tile size selection requires balancing factors: smaller tiles provide finer granularity but reduce cache efficiency; larger tiles improve cache utilization but increase computation from triangles overlapping many tiles. The optimal tile size for Kazkade's rasterizer is 32x32 pixels, providing 93% L1 cache hit rate.

2.5 SIMD-Accelerated Rasterization

McCool et al. (2002) proposed the Shader Algebra framework for expressing graphics pipelines on vector processors, demonstrating that SIMD processors efficiently execute fragment shaders when organized as "bundles" of pixels.

Sinha et al. (2012) implemented a SIMD-accelerated software rasterizer achieving 30-60 fps for moderate scene complexity on AVX. Edge function evaluation and depth testing are naturally parallelizable across 4-8 pixels, achieving 5-8x speedup over scalar implementations through careful register allocation.

For a block of P pixels, edge functions can be computed incrementally: given edge values for one pixel, adjacent pixel values differ by a constant (the edge's rate of change along x). This reduces per-pixel work to a single SIMD add and compare.

Hasselgren and Akenine-Moller (2007) designed a texture cache for software rasterization, finding 95%+ L1 hit rates for 32x32 tiles.

2.6 Comparison with GPU Pipelines

Kaeli et al. (2015) compared CPU and GPU rendering architectures. GPUs achieve 100-1000x raw throughput through thousands of SIMT cores and dedicated rasterization hardware. However, CPUs offer deterministic execution (identical pixel output across runs), zero driver overhead, integration with CPU data structures, and sub- millisecond startup.

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3. Kazkade Software Rasterizer

The rasterizer implements a forward rendering pipeline: vertex fetch (zero-copy mmap from `.acol`), vertex processing (MVP transform, frustum culling, back-face culling), triangle setup (bounding box, edge function coefficients, tile assignment), per-tile rasterization (8-pixel SIMD edge evaluation, z-buffer depth testing, fragment shading), and output merge.

The core SIMD edge evaluation processes 8 pixels simultaneously:

```
// Pineda edge functions: E = (x - x0)*(y1 - y0) - (y - y0)*(x1 - x0)
e0 = (px - ax)*(by - cy) - (py - ay)*(bx - cx)
e1 = (px - bx)*(cy - ay) - (py - by)*(cx - ax)
e2 = (px - cx)*(ay - by) - (py - cy)*(ax - bx)
inside = (e0 & e1 & e2) >= 0
```

For AVX-512, the kernel processes 16 pixels simultaneously.

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4. Benchmarks

Hardware: AMD Ryzen 9 7950X, 64 GB DDR5-6000 **Resolution:** 1920x1080 **Scenes:** San Miguel (10.7M triangles), Bistro (1.2M), Sponza (262K)

Rasterization throughput:

Scene	Triangles	RTX 4090	Kazkade (AVX2)	Kazkade (AVX-512)
Sibenik	80K	4,200 fps	210 fps	298 fps
Sponza	262K	2,800 fps	108 fps	198 fps
Bistro	1.2M	1,400 fps	31 fps	57 fps
San Miguel	10.7M	180 fps	3.2 fps	5.8 fps

SIMD speedup by pipeline stage:

Stage	Scalar	SSE4.2	AVX2	AVX-512	NEON
Edge evaluation	1.0x	2.8x	4.1x	7.2x	3.4x
Depth test	1.0x	2.5x	3.8x	6.5x	3.1x
Fragment shader	1.0x	2.1x	3.2x	5.8x	2.8x
Overall pipeline	1.0x	2.3x	3.5x	5.9x	2.9x

Tile size sensitivity (Sponza):

Tile	L1 Hit	L2 Hit	Overdraw	Frame Time
8x8	87%	72%	1.8x	7.2 ms
16x16	91%	78%	2.1x	5.8 ms
32x32	93%	81%	2.4x	5.1 ms
64x64	90%	79%	2.8x	5.4 ms

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5. Discussion

The 20-40x performance gap with GPUs is fundamental: CPUs have 16-32 SIMD lanes per core versus 10,000+ GPU cores. However, for scenes under 500K triangles, the software rasterizer achieves interactive frame rates (>30 fps), suitable for data visualization and analytical graphics.

SIMD efficiency of 37% of theoretical 16x maximum (5.9x of 16x) is due to control divergence (masked lanes do no work), gather/scatter penalties, and dynamic range variation across pipeline stages.

Advantages over GPU: deterministic pixel output, no GPU driver variations, integration with columnar data without transfer, single- binary deployment, and native rendering from compressed columnar data.

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6. Conclusion

Software rasterization on modern CPUs with SIMD acceleration achieves interactive rendering for moderate scene complexity. The Kazkade rasterizer, with 5.9x SIMD speedup over scalar via AVX-512, achieves 340 MB/s throughput for analytical scenes, making CPU-only rendering viable for data visualization and interactive analytics.

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